# Quantum Most-Significant Digit-First Addition

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Abstract—In recent years, quantum computers have attracted extensive research interests due to their potential capability of solving problems which are not easily solvable using classical computers. In parallel to the constant research aiming at the physical implementation of quantum processors, there is another branch of research developing quantum algorithms for reallife applications, many of which need to perform arithmetic operations. As one of the most important operations, quantum addition has been adopted in Shor's algorithm, quantum linear algebra algorithms and various quantum machine learning applications. Since precision is always a non-trivial issue to determine during the computation, most-significant digit-first quantum addition can be a fundamental operation for variable precision computing. Therefore, this paper proposes the first quantum adder circuit that is able to compute from the mostsignificant digits, which demonstrates the advantages over the state-of-the-art quantum adders requiring carry propagation to produce results from least-significant digits. We first present a review of quantum addition circuits design, and then propose a novel method to implement quantum most-significant digit-first adders. Scalability and quantitative comparisons for different quantum full adder, quantum carry-ripple adder and quantum most-significant digit-first adder circuits have been investigated, where all circuits are implemented on IBM Qiskit SDK.

## I. INTRODUCTION

Quantum computing (QC) has received extensive attention in developing the first large-scale quantum computer, which has already become one of the most promising technology for future computer systems [1], [2]. As McKinsey consulting estimated, the quantum computing industry was worth \$507.1 million in 2019, and may exceed \$65 billion by 2030 [3]. Since a desired scale fault-tolerant quantum computer still remains unreachable, dealing with noise errors in current Noisy Intermediate Scale Quantum (NISQ) technology is of high significance [4]. Efforts are required to build functionally correct quantum circuits to overcome quantum operation errors and quantum coherence errors in the NISQ era. One popular solution nowadays is to design efficient quantum arithmetic circuits, where one of the fundamental components is the adder circuit [5]–[9].

The main purpose of this paper is to design an efficient method for quantum addition, which combines quantum gate theory with traditional most-significant digit-first (MSDF) and lest-significant digit-first (LSDF) arithmetic algorithms. Based on the quantum development platform provided by IBM

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Qiskit [10], we aim to provide a library of quantum arithmetic operators, including different quantum adder designs.

The main model of quantum computing is related to quantum circuit design, in which logical gates are replaced with quantum ones [11]. Quantum gates must be reversible which are required to obey the laws of quantum physics. Therefore, reversibility not only results in energy saving but also becomes a fundamental requirement of quantum computing. Circuits for performing the quantum addition are especially relevant with several quantum algorithms, such as Shor's algorithm, that achieve a speedup over the best known classical methods. Shor's algorithm is a famous quantum algorithm used to factorise numbers and compute discrete logarithms in polynomial time [12]. Its classical counterparts are cryptographic protocols such as the RSA cryptosystem [11] or Diffie-Hellman key exchange [13], leading to highly non-trivial actual implementations as the data size increasing. In the past two decades, a wide variety of reversible quantum adder circuits have been presented. However, it is not always easy to analyze or compare them due to the following two main reasons:

- Lack of consistent metrics used to evaluate each design.
- Lack of detailed design parameters discussion and comparison.

Therefore, we present a brief review of quantum adder circuit designs, with the hope to find out how to choose a right quantum adder circuit if we do not have much information about quantum arithmetic, and how we can optimise a quantum circuit design.

While employing arithmetic operators to solve a particular problem, how to choose an appropriate operation precision is usually a difficult problem. In classical computing, designers generally use finite-precision arithmetic, most of which operate least-significant bits first [14]. The precisions of such implementations are either under- or over-budgeted for the computation of a result to a particular accuracy [15]. As an alternative solution, use of MSDF arithmetic helps us to perform variable-precision computing [16]. After reviewing the existing quantum adder circuits, all of them belong to LSDF fashion. Therefore, in this paper, we investigate the design methods of MSDF quantum addition. Scalability and quantitative comparisons in terms of qubit usage, implementation cost (*i.e.* quantum gate cost), and latency (*i.e.* circuit depth) of our proposal are discussed.

The contributions of this paper are summarised as follows:



Fig. 1: Symbols and transformation of some elementary quantum gates.

- We present a review of the state-of-the-art quantum adder circuit designs, and provide consistent comparisons for different quantum addition designs.
- We propose the first design method for quantum MSDF adder circuits which can be used for variable precision calculations.
- A library of quantum circuit implementations for quantum LSDF and MSDF addition.
- Quantitative comparisons and scalability analysis for quantum full adder, carry-ripple adder and MSDF adder circuits are provided, showing the design space exploration on qubit usage, implementation cost and latency.

## II. BACKGROUND

## A. Basic Elements of Quantum Circutis

A quantum circuit is made up of elementary quantum gates, such as Hadamard gate (H), phase gate (S), NOT (X) and Controlled-NOT (CNOT) or CX gate [17]. These elementary quantum gates belong to Clifford group, because any gate in this group can be produced by combinations of Hadamard, phase and CNOT gates [18]. Figs. 1a, 1b and 1c show the symbolic description of exemplar Clifford gates. However, in most fault-tolerant quantum computing architectures, the most difficult quantum gates to produce are non-Clifford gates [18], such as Toffoli gate [19] and Peres gate [20]. These are some common quantum gates composed of Clifford and non-Clifford quantum gates. Each of them represents a state transformation on some qubits and has a corresponding transformation matrix, which is a unitary matrix. Figs. 1d, 1e, 1f and 1g show the symbolic description of these non-Clifford gates.

Fig. 1a illustrates a NOT gate which is a 1-qubit gate, used to invert the state of the qubit. The CNOT gate is a 2-qubit quantum gate, as is shown in Fig. 1b, where one of these



Fig. 2: Binary MSDF adders. Left: serial. Right: parallel [22].

qubits is a control qubit and another one is a target qubit whose state will be inverted if and only if the state of the control qubit is  $|1\rangle$ . Hadamard gate, illustrated in Fig. 1c, is used to create a superposition given a basis state, where  $|0\rangle$  can be mapped to  $\frac{|0\rangle+|1\rangle}{2}$  and  $|1\rangle$  to  $\frac{|0\rangle-|1\rangle}{2}$ . In Fig. 1d, the Toffoli gate is a quantum gate with 3 qubits. Two of these qubits are control qubits and the third one is a target qubit whose state will be inverted if and only if the state of control qubits is  $|11\rangle$ . Toffoli gate is composed of 5 elementary quantum gates. Fig. 1e indicates NG gate which is built by 1 CNOT gate, 1 NOT gate, 2 Toffoli gates and 1 Swap gate. The total number of elementary quantum gates consumed is 13. As is shown in Fig. 1f, the Peres gate is also a 3-qubit gate, which works similar to the Toffoli gate in combination with a CNOT gate. Peres is composed of 4 elementary gates. Square-root of CNOT gate and its hermitian are shown in Fig. 1g, used to simplify the quantum logic for quantum circuit implementations [8].

To gain information about the state of qubits after being transformed by a quantum gate, measurement is needed. The act of measurement collapses the state of qubits, which is called the observer effect [21]. When a qubit is measured, its superposition state will collapse into a well-defined state of either  $|0\rangle$  or  $|1\rangle$ . It should be noted that it is the state of the qubit rather than the qubit itself that is changed. Therefore, the qubit can be reused with a well-defined state.

### B. Most-Significant Digit-First Addition

Most-significant digit-first arithmetic is seeing renewed interest owing to the emergence of domain-specific hardware accelerators for high-performance computing applications, particularly in the field of machine learning [23]. Arithmetic algorithms have two typical operation modes, *i.e.* LSDF and MSDF [22]. In LSDF computing, operand and result digits are applied from the least-significant end, such as traditional addition and multiplication. MSDF computing instead applies operand and result digits from the most-significant end. A de facto standard for MSDF arithmetic is online arithmetic [22]. Users can choose both digit-serial and -parallel online operators in their design. For example, digit-serial online adder is presented in Fig. 2 (left), while duplication of the serial adder M times and the removal of its registers lead to the creation of a *M*-digit parallel online adder, as shown in Fig. 2 (right) [22]. Even though carrys are delivered at the LSD end and generated at the MSD end in online adders, there is no carry chain; the critical path lies across two full adders (FAs) [22]. This implies online adder's suitability for the construction of more complex online operators, such as multiplication and division. In this paper, we employ the traditional MSDF addition algorithms to build quantum MSDF adder circuits, with the optimizations of reducing the usage of qubits, garbage qubits and quantum gates.

## **III. REVIEW OF QUANTUM ADDITION CIRCUITS**

A full adder (FA) in a classical circuit can be used to add three classical bits with an input carry bit and two operands. FA is a fundamental mathematical calculation circuit in classical computers, characterized by

$$Sum = A \oplus B \oplus C$$
$$Carry = AB \oplus AC \oplus BC$$

In quantum computing, quantum gates are used to replace logical gates [24] to form a quantum full adder (QFA). The aforementioned discussions briefly introduced the functionality of different quantum gates. Given the available quantum gate models, we can construct a quantum full adder circuit. There are several solutions that allow performing addition in an efficient way. In this section, we classified quantum adder circuits by the number of qubits consumed.

# A. Design of 7-qubit Quantum Full Adder



Fig. 3: Design of 7-qubit quantum full adder [5].

Mazumder presented a reversible quantum adder circuits by proposing a Khan Gate (NG), *i.e.* the  $4 \times 4$  parity preserving reversible gate [5]. As shown in Fig. 3, Khan Gate is implemented using quantum gate CNOT, NOT, positive and negative controlled Toffoli gate and Swap gate. This structure is composed of 7 qubits and the number of garbage qubits is 5. Since this adder circuit contains 3 NG gates, the number of elementary quantum gate cost is 15.

## B. Design of 5-qubit Quantum Full Adder

Fig. 4 shows a QFA circuit with 5 qubits, including two input data qubits, one input carry qubit, one output carry qubit, and one addition result qubit [6]. This structure has 3 garbage qubits and its gate cost is 7. Since three input qubits can be garbage qubits [25] in the end of the quantum circuit, these qubits can also be used as output qubits. In other words, input qubits can be reused to perform output qubits.



Fig. 4: Design of 5-qubit quantum full adder [6].



Fig. 5: Design of 4-qubit quantum full adder based on Peres gates [7].

## C. Design of 4-qubit Quantum Full Adder

1) Use of Peres Gates: Fig. 5 shows a quantum adder circuit with 4 qubits, where the third qubit is served as input qubit  $|C_{in}\rangle$  and output qubit  $|Sum\rangle$  at the same time. This architecture is called PFAG, employing two Peres gates [7]. Since this structure is composed of 2 Peres, the gate cost is 2, along with 2 garbage qubits.

2) Use of Controlled Square Root of X Gate: The square root of CNOT gate, namely V gate, owes its name to the following properties:

$$\sqrt{X} \cdot \sqrt{X} = X \tag{1}$$

$$\sqrt{X^{\dagger}} \cdot \sqrt{X^{\dagger}} = X \tag{2}$$

$$\sqrt{X} \cdot \sqrt{X^{\dagger}} = I \tag{3}$$

where the dagger of a matrix is obtained by conjugating and transposing the matrix [17]. The conjugate matrix of a matrix is obtained by performing the complex conjugate of each element. Possible implementations for the controlled square root of CNOT and for its application of quantum addition are shown in Fig. 6. With the use of V gates, the number of quantum gates is reduced for an adder circuit design. As is shown in Fig. 6, the quantum adder circuit is made up of only 6 gates, and consumes 4 qubits and 2 garbage qubits, respectively.



Fig. 6: Design of 4-qubit quantum full adder based on V gates [8]. The  $V^+$  gate is Hermitian of V gate.



(b) 3-CNOT version

Fig. 7: Design of 4-qubit quantum full adder based on qubit state reuse [9].

3) Qubit State Reuse: Cuccaro et al. proposed a novel carry-ripple adder with less qubit usage [9]. When bit-width of input data is 1, the carry-ripple adder equals to a full adder in which two garbage qubits maintain their initial state, *i.e.* qubit state reuse. Two different structures are proposed in this work, illustrated in Fig. 7. In the 2-CNOT version, 4 CNOT gates and 2 Toffoli gates are contained. Therefore, the number of elementary quantum gates is 14. For the 3-CNOT version, 2 NOT gates, 6 CNOT gates, and 2 Toffoli gates are contained. Although the number of elementary quantum gates is 18, which is larger than the former design, it admits greater parallelism.

4) Reduction of Non-Clifford Gates: Gigney reduced the number of non-Clifford gates used to perform a quantum addition, because non-Clifford gates dominate the cost of quantum computation [26]. Gigney followed the work mentioned in [9], and built a temporary logical-AND operator to replace Toffoli gate in adder circuits. As is shown in Fig. 8, this method aims to design quantum adder circuits with fewer non-Clifford gates.



Fig. 8: Design of 4-qubit quantum full adder by reducing non-Clifford gates usage [26].

## IV. DESIGN OF QUANTUM MSDF ADDITION

Using classic online addition algorithm and the state-ofthe-art quantum adder circuits as a starting point, we now describe the construction of quantum MSDF addition capable of performing results in the left-to-right mode.

# A. Proposed Architecture

As is shown in Section II, an MSDF adder makes use of full adders to add digits of inputs. Therefore, we now investigate the construction of quantum MSDF adders based on different quantum full adders, in order to provide some design space exploration for a balanced design of quantum adder circuits. In quantum MSDF addition, the FAs are substituted with QFAs. Mirrored to classical parallel MSDF addition in Fig. 2, the length of input data of the proposed quantum MSDF addition is p, which corresponds to 2p qubits using *de facto* radix-2 signed-digit number representation [22].

We propose three design strategies for quantum adder circuits design. The first strategy is called direct quantum addition implementation. Before the actual implementation, we first build a library of quantum LSDF adders (*i.e.* QFAs), so that designers can instantiate a QFA given a particular specifications in terms of gate cost, latency (circuit depth), and the number of qubits required.

Due to the scarce qubit resource, we further investigate an optimised design method for qubit-efficient quantum circuits. Versus chaining the arithmetic operators directly, we analyse the data dependencies in the data flow graph, extracted from digital circuits. When an operator's input states stays unchanged at the output, we can employ the qubit-reuse QFA, as was elaborated in Section III.C, to reduce the total number of qubits for quantum MSDF adder. This design optimisation will be discussed and demonstrated in Section.V.B.

Apart from the optimisation target of qubit usage, there are other factors which can be considered for design space exploration of quantum circuits design, such as implementation cost (*i.e.* the number of quantum gates), latency (*i.e.* circuit depth) and computation accuracy [26]. Although this paper focuses on addition, we consider our main conceptual contribution to other quantum arithmetic operations and quantum algorithms.

## B. Quantum MSDF Adder Circuits

We first present a direct implementation of a quantum MSDF adder. Herein we choose to use 7-qubit QFAs as a baseline, and the architecture of a quantum MSDF adder is shown in Fig. 9, where the red dotted part is a basic unit of this quantum MSDF adder circuits and can be duplicated in the implementation. In this unit, the number of qubits, quantum gates and garbage qubits are 12, 33 and 10, respectively. Consider that input data is represented by *p*-bit precision, there will be *p* units. At the bottom of this circuit, there will be 2 additional qubits used for initial carry-in values. Consequently, this *p*-bit quantum MSDF adder requires 12p+2 qubits, 33p quantum gates (including 6 swap gates) and 10p garbage qubits.

In order to reduce the number of qubits used in quantum MSDF adder, we further employ 5-qubit QFAs and 4-qubit QFAs to construct quantum MSDF adders. Fig. 10 represents a design with 5-qubit QFAs, where 8p+2 qubits, 17p quantum gates and 6p garbage qubits are used.

Since there have been several 4-qubit QFAs available, we can choose the most appropriate QFA to construct a quantum



Fig. 9: Quantum MSDF Adder Based on 7-qubit QFA [5].

MSDF circuit with the implementation cost and accuracy tradeoff. Fig. 11 employed the Peres-based QFA to construct quantum MSDF adder. For a p-bit adder, it requires 6p + 2qubits, 7p quantum gates and 4p garbage qubits. When we use V-gate based QFA to construct a p-bit quantum MSDF adder, the quantum gates usage increases to 15p, and the number of qubits and garbage qubits usage are the same as the Peres-based implementation. However, the Peres gate can be made up of 3 V-gate and a CNOT gate, therefore, this design costs fewer elementary quantum gates than Peres-based implementation. Moreover, quantum MSDF adders implemented following Cuccaro *et al.*'s proposal require 6p + 2 qubits, 17pquantum gates and 4p garbage qubits. To achieve an areaefficient quantum MSDF adder, we should reduce the usage of non-Clifford gates, as suggested by Gigney [26]. Following the principles to optimise non-Clifford gate usage [26], Fig. 14 shows a circuit design with only 6p + 2 qubits, 15p quantum gates and 4p garbage qubits. Note that the number of gates represents the summation of different quantum gates used. A non-Clifford gate will be composed of multiple Clifford and non-Clifford gates, resulting in more elementary quantum gates usage. The detailed classification will be addressed in Tables II and III in Section V.

## V. EVALUATION

## A. Experimental Setup

In this section, a series of experiments are implemented in the quantum development platform provided by IBM Qiskit [10]. Some metrics are used to compare different designs. Since the number of qubits in the state-of-the-art quantum computers is several dozens, qubit resource is actually extremely scarce. Therefore, the number of qubits is the most important metric to characterize the superiority of a quantum circuit design [4]. The cost of quantum gates is



Fig. 10: Quantum MSDF Adder Based on 5-qubit QFA [6].

also used to show the total usage of quantum primitives [20]. Finally, the number of garbage qubits which can be reused in later quantum circuits and circuit depth which is related to latency are discussed.

# B. Scalability and Quantitative Comparisons for Different QFAs

In Section III, we reviewed the state-of-the-art QFA circuits using different design strategies. Table I shows the experimental comparison results of different QFA circuit designs. The data is reported by reproducing the designs on IBM Qiskit platform. Considering the fact that qubits are the most scarce resource in quantum computers, 4-qubit QFAs are more piratical for real-world quantum applications. Even though there are four 4-qubit QFAs available, each is performed by different quantum gate models. For a specific application, we should choose an appropriate gate model to build 4-qubit QFAs [26].

To further demonstrate the superiority of QFAs, we also employ these QFAs to construct a quantum carry-ripple adder (QCRA). Carry-ripple addition (CRA) is one of the mostly used classical LSDF addition algorithms [22]. CRA is made

TABLE I: Comparison of Binary Quantum Full Adder

Design methods	# qubits			#	gates			#	Circuit depth						
		NOT	CNOT	Toffoli	Peres	V	Logical AND	# garbage qubits	NOT	CNOT	Toffoli	Peres	V	Logical AND	
Mazumder et al. [5]	7	3	3	6	0	0	0	5	3	3	6	0	0	0	
Sohel et al. [6]	5	0	5	2	0	0	0	3	0	4	2	0	0	0	
Islam [7]	4	0	0	0	2	0	0	2	0	0	0	2	0	0	
Biswas et al. [8]	4	0	2	0	0	4	0	2	0	2	0	0	4	0	
Cuccaro et al. [9]	4	0	5	2	0	0	0	2	0	4	2	0	0	0	
Gidney [26]	4	0	5	0	0	0	1	2	0	3	0	0	0	1	

TABLE II: Comparison of carry-ripple adders with different QFAs

Benchmark	QFA methods	# qubits			#	gates			# garbage qubits	Circuit depth						
			NOT	CNOT	Toffoli	Peres	V	Logical AND		NOT	CNOT	Toffoli	Peres	V	Logical AND	
QCRA-1	Mazumder et al. [5]	6p+1	3p	3p	6р	0	0	0	5p	2p+1	1	4p+2	0	0	0	
QCRA-2	Sohel et al. [6]	4p+1	0	5p	2p	0	0	0	3p	0	2p+2	p+1	0	0	0	
QCRA-3	Islam [7]	3p+1	0	0	0	2p	0	0	2p	0	0	0	p+1	0	0	
QCRA-4	Biswas et al. [8]	3p+1	0	2p	0	0	4p	0	2p	0	p+1	0	0	2p+2	0	
QCRA-5	Cuccaro <i>et al.</i> [9] $(p \ge 2)$	2p+2	2p-4	5p-3	2p-1	0	0	0	p+1	0	5	2p-1	0	0	0	
QCRA-6	Gidney [26]	3p+1	0	5p	0	0	0	2p	2p	0	3p	0	0	0	2p	

TABLE III: Comparison of quantum MSDF adders with different QFAs

Benchmark	QFA	# qubits			#	gates			# garbage qubits	Circuit depth					
	methods		NOT	CNOT	Toffoli	Peres	V	Logical AND		NOT	CNOT	Toffoli	Peres	V	Logical AND
QMA-1	Mazumder et al. [5]	12p+2	9p	6р	12p	0	0	0	10p	7	5	11	0	0	0
QMA-2	Sohel et al. [6]	8p+2	3p	10p	4p	0	0	0	6р	1	6	3	0	0	0
QMA-3	Islam [7]	6p+2	3p	0	0	4p	0	0	4p	2	0	0	4	0	0
QMA-4	Biswas et al. [8]	6p+2	3p	4p	0	0	8p	0	4p	2	2	0	0	7	0
QMA-5	Cuccaro et al. [9]	6p+2	3p	10p	4p	0	0	0	4p	2	8	4	0	0	0
QMA-6	Gidney [26]	6p+2	3p	10p	0	0	0	2p	4p	2	6	0	0	0	2

up of an array of FAs. In QCRA implementation, FAs are replaced by QFAs. Table II elaborates the design parameters for different QCRA circuits, including the number of qubits, gates and garbage qubits. We can see that QCRA-5 using Cuccaro *et al.*'s proposal [9] demonstrates the superiority in terms of the number of qubits and garbage qubits consumption over all other QCRA designs. In terms of implementation cost, QCRA-6 employs logical AND [26] units to replace the non-Clifford gates, thereby leading to much reduction in the gate consummation. It is also noted that different QCFAs have different circuit depth, which leads to different latency during the computation. Therefore, the realisation of low-depth quantum circuits is an interesting optimisation direction, a task we left for a future work.

We remark that some special quantum gates are not con-

tained in Qiskis, therefore we replaced them with the combination of other general quantum gates. For example, there is no Peres gate in Qiskit circuit library [27]. However, Peres gate can be substituted by using a Toffoli gate and a CNOT gate [28].

## C. Evaluation of Quantum MSDF Adders

In Section IV, principles of quantum MSDF adders have been introduced. Table III shows the comparisons of different quantum MSDF adder (QMA) circuits. Similar findings can be found with respect to the discussions for QFAs and QCRAs. Quantum MSDF adders based on Mazumder *et al.*'s [5] and Sohel *et al.*'s [6] QFAs consume  $2.0 \times$  and  $1.3 \times$  more qubits and  $2.5 \times$  and  $1.5 \times$  more garbage qubits versus the other MSDF adders using 4-qubit QFAs. Furthermore, we can find



Fig. 11: Quantum MSDF Adder based on 4-qubit QFA using Peres gates.



Fig. 12: Quantum MSDF Adder based on 4-qubit QFA using V gates.

that quantum MSDF adders following Biswas *et al.*'s [8], Islam *et al.*'s [7] and Cuccaro *et al.*'s QFAs consume more elementary quantum gates because each Toffoli, Peres, and Vgate is composed of multiple elementary quantum gates. If we only consider the number of qubits and implementation cost, quantum MSDF adder based on Gidney's proposal [26], named QMA-6, would be an appropriate choice. However, Gidney's



Fig. 13: Quantum MSDF Adder based on qubit state reuse.



Fig. 14: Quantum MSDF adder based on less non-Clifford gates usage.

QFAs introduced phase errors and have to assume that the intermediate quantum gates are not sensitive to these phase errors [26]. This issue would result in a potential security vulnerability to the overall system.

# D. Evaluation of Quantum Adder Tree

Since adder tree is one of the most widely used circuits in quantum machine learning and quantum image processing [29], herein we investigate the scalability of qubit-efficient quantum adder tree circuits. In classical LSDF adder tree, we usually need to analyze the precision of each layer, thereby only allowing finite-precision addition. Use of MSDF arithmetic provides a possible solution to overcome the predetermination of precision in adder trees. We can reuse the MSDF arithmetic circuits to calculate less significant bits as time grows. We chose the QMA-6 to construct a quantum adder tree circuit, because it consumes the least qubits and quantum gates among all implemented quantum MSDF adders. Consider that there are  $2^n$  *p*-bit numbers to calculate, a *n*level quantum adder tree is needed. The number of qubits and quantum gates used in this quantum adder tree circuit scale linearly with the precision p and exponentially with n, in the complexity of  $\mathcal{O}(2^n p)$ .

## VI. CONCLUSIONS

In this paper, we analysed the design parameters of the state-of-the-art quantum full adder circuits. Our evaluation adopts qubits, quantum gates and circuit depth as key metrics for consistent comparisons among different quantum adder designs. After a quantitative investigation on previous quantum adder designs, we observe that all of them require the carry chains to generate results from least-significant digits. Therefore, we proposed the design method of quantum MSDF adders which can generate results from most-significant digits. All quantum circuits are evaluated on the IBM Qiskit SDK. Scalability and quantitative comparison for quantum full adder, quantum carry-ripple adder, quantum MSDF adder circuits were provided in order to analyse their applicability. In the future, we will extend our arithmetic library to more complex arithmetic operations. We are also keen to adapt our proposed approach in quantum machine learning algorithms, for which we expect to achieve substantial performance gains due to our qubit-efficient arithmetic circuits.

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